IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	§	Attorney Docket No. 2002-0210
	§	24061.475
Chao-Cheng Chen, et al.	§	
	§	Customer No. 42717
Serial No. 10/714,304	§	
	§	Group Art Unit: 2823
Filed: November 14, 2003	§	
	§	Examiner: Michelle Estrada
For: Dual Damascene Process Flow for Porous Low-K Materials	§	
	§	
	§	

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BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
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This Brief is submitted in connection with an appeal from the final rejection of the Examiner, dated August 23, 2005, finally rejecting claims 1, 4-8, and 10-14.

REAL PARTY IN INTEREST

The real party in interest is Taiwan Semiconductor Manufacturing Company, a company having a principal place of business at Hsin-Chu, Taiwan, Republic of China.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and no related interferences regarding the above-identified patent application.

STATUS OF CLAIMS

Claims 1, 4-8, and 10-14 are pending, stand finally rejected, and are on appeal here. Claims 2, 3, 9, and 15-50 have been allowed. Claims 1-50 are set forth in Appendix A attached hereto.

STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendments were made after the Final Office Action was filed August 23, 2005.

SUMMARY OF THE INVENTION

The present invention, as set forth in independent claim 1, relates to a method of forming a dual damascene opening. A structure having an overlying exposed conductive layer formed thereover is provided (Page 5, Lines 6-7, and Lines 14-15). A dielectric layer is formed over the exposed conductive layer (Page 6, Lines 4--9). An anti-reflective coating layer is formed over the dielectric layer (Page 6, Lines 10-13). The anti-reflective layer and the dielectric layer are etched using a via opening process to form an initial via exposing a portion of the conductive layer (Page 6, Lines 14-18; Page 7, Lines 16-19; : and element 11, Figure 3). A protective film portion is formed over at least the exposed portion of the conductive layer. The protective film portion is comprised of the elements C and H (Page 8, Lines 1-5; and Figure 4, element 24). The anti-reflective coating layer and the dielectric layer are patterned to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening (Figure 2, elements 16' and 18'; Page 7, Lines 8-11; and Page 9, Lines 1-4).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1, 4-8, and 10-14 stand rejected under 35 U.S.C. § 103(a) over U.S. Patent Application No. 2004/0166669 to Saito ("Saito") in view of U.S. Patent Application No. 2003/0054629 to Kawai et al. ("Kawai").

ARGUMENT

ISSUE 1

The first issue for the Board's consideration is whether claims 1, 4-8, and 10-14 are unpatentable under 35 U.S.C. §103(a) over Saito in view of Kawai.

As detailed below, Applicants believe that the Examiner has improperly applied the combination of references to the claims. More specifically, it is Applicants' belief that the Examiner cannot factually support a prima facie case of obviousness with respect to the rejected claims because the references, even when combined, fail to teach or suggest the claimed subject matter.

Claim 1

Applicants traverse the rejection of these claims on the grounds that the references are defective in establishing a prima facie case of obviousness. It is well settled that, in order to reject a patent application for obviousness, the prior art reference must teach or suggest all of the claimed limitations. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, all words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Applicants respectfully submit that even if combined, Saito and Kawai clearly do not teach or suggest the limitations of claim 1.

With respect to the improper application of Saito and Kawai, Applicants submit that neither Saito nor Kawai, separately or in combination, teach or suggest all of the elements of claim 1 as required by MPEP § 2143. Applicants traverse the rejection of this claim on the grounds that the references are defective in establishing a prima facie case of obviousness.

Claim 1 recites:

> 1. A method of forming a dual damascene opening, comprising the steps of:
> providing a structure having an overlying exposed conductive layer formed thereover;
> forming a dielectric layer over the exposed conductive layer;
> forming an anti-reflective coating layer over the dielectric layer;
> etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer, the protective film portion being comprised of the elements C and H; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) <u>must teach or suggest all the claim limitations</u>.

The MPEP § 2142 provides:

> ... The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness...

Additionally, MPEP states the following:

> MPEP 2111 Claim Interpretation; Broadest Reasonable Interpretation
>
> CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE INTERPRETATION
>
> During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification...The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach..." (in part)
>
> MPEP 2111.01 Plain Meaning:
>
> "PLAIN MEANING" REFERS TO THE MEANING GIVEN TO THE TERM BY THOSE OF ORDINARY SKILL IN THE ART
>
> When not defined by applicant in the specification, the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art. (in part).

It is submitted that, in the present case, the Examiner has not factually supported a prima facie case of obviousness.

The Final Office Action alleges that Saito describes "forming a protective film portion over at least the exposed portion of the conductive layer." Applicants respectfully disagree. The Examiner alleges that the description provided by Saito of filling a via hole with a conductive polymeric member is sufficient to disclose the subject claim limitation of "forming a protective film portion over at least the exposed portion of the conductive layer." That is, the Examiner has interpreted a protective film, as described in the subject application, as a via fill, as described by Saito (See Final Office Action dated 8/23/2005, Pages 2-3).

Applicants submit that the Examiner's interpretation of a "film," as taught by the subject application, as a "conductive polymeric member," as described by Saito, is outside the broadest reasonable interpretation of "film."

With regard to the "conductive polymeric member," as disclosed by Saito, Applicants note the following passage of Saito:

> Subsequently, as shown in FIG. 1C, a *conductive polymeric member 4* is *formed* only *in the via hole 3* by electrolysis. The burying of the conductive polymeric member 4 is stopped at a top surface of the interlayer insulating film 2 by adjusting the time of the electrolysis. For example, the conductive polymeric member 4 is made of a conductive polymer such as an aniline, pyrrole, or thiophene polymer. The pyrrole polymer is formed by electrolyzing a pyrrole monomer of 0.14 mol/l and a p-toluenesulfonate of 0.05 mol/l in a propylene carbonate solution as an electrolyte.

Saito, Paragraph 0029 (emphasis added).

Thus, conducive polymeric member 4 comprises a via fill and is in no manner described or shown by Saito as a "film."

With regard to the usage of the term "protective film", Applicants note the following passages of the subject application:

> As shown in FIG. 4, *a protective film* is *deposited* over the structure of FIG. 3 to form protective film portions 22 over the patterned ARC layer 18' and a *protective film portion 24 over the exposed portion* 11 of metal layer 12.
>
> *Protective film portions 22, 24* are preferably *comprised* of an *organic chemical vapor deposition (CVD)* film including the elements C, O and H such as C_xH_y and specifically such as, for example, C_2H_4 or C_2H_6, as will be used for illustrative purposes hereafter, and protective film portion 24 is used to protect the otherwise

> exposed metal portion thereunder to prevent damage to the metal during subsequent processing.
>
> Organic CVD film portion 24 is formed to a thickness of preferably from about 50 to 2000 Å and more preferably 200 to 1500 Å.

Subject Application, Page 8, Lines 3-13 (*emphasis added*).

Thus, the subject application makes clear that the characterization of the protective film is made in a conventional sense of the term "film" including the film formation mechanism, e.g., CVD.

Thus, it is clear that the Examiner's interpretation of a "protective film" as a "conductive polymeric member" as described by Saito is not consistent *with the subject specification description of the protective film.* For at least this reason, the interpretation of a protective film as a polymeric member via fill is outside the broadest reasonable interpretation of the claim language afforded by the subject application. Accordingly, the interpretation of the claimed protective film a polymeric member described by Saito is inconsistent with MPEP 2111. For at least this reason, Saito fails to describe or suggest "forming a protective film portion over at least the exposed portion of the conductive layer" as described in the subject application and clearly recited in claim 1.

Moreover, an interpretation of the claim language according to the plain meaning of the claim terms fails to render claim 1 obvious. For example, the following common definitions of *film* are as follows:

> film:
> 1 a : a thin skin or membranous covering
> 2 : a thin covering or coating <a *film* of ice>
> 3 a : an exceedingly thin layer
> Merriam Webster online.

Merriam Webster online.

Thus, as dictionary definitions of the subject term indicates, interpretation of the conductive polymeric member as a film is inconsistent with the plain meaning given to the term "film" as the conductive polymeric member via fill described by Saito is not shown or otherwise characterized in any manner consistent with the plain meaning of the term film. For at least this reason, Saito fails to describe or suggest "forming a protective film portion over at least the

exposed portion of the conductive layer" as described in the subject application and clearly recited in claim 1.

Moreover, Applicants submit that no reputable reference exists in the art that refers to a via fill as a "film," and thus interpretation of a protective film as a via fill is inconsistent with the interpretation that those skilled in the art would reach and is thus contrary to MPEP 2111. For at least this reason, Saito fails to describe or suggest "forming a protective film portion over at least the exposed portion of the conductive layer" as described in the subject application and clearly recited in claim 1.

For the reasons discussed above, Saito and Kawai are insufficient to provide a *prima facie* case of obviousness with regard to the claim 1 limitations.

Claims 4-8 and 10-14 depend from, and further limit claim 1. Therefore, the same distinctions between Saito and Kawai and the claimed invention in claim 1 apply for claims 4-8 and 10-14. For at least this reason, Saito and Kawai do not render claims 4-8 and 10-14 *prima facie* obvious.

II. Conclusion

Accordingly, it is respectfully submitted that the references alone or in combination do not disclose or suggest the subject matter of claims 1, 4-8, and 10-14.

For all of the foregoing reasons, it is respectfully submitted that claims 1, 4-8,and 10-14 be allowed. A prompt notice to that effect is respectfully requested.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer, the protective film portion being comprised of the elements C and H; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

2. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer, the protective film portion being comprised of the elements C and H; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening, wherein the structure includes a silicon substrate or a germanium substrate; the conductive layer is comprised of copper, aluminum, gold or silver; the dielectric layer is comprised of the elements Si, O, C and/or H such as SiOCH; and the anti-reflective coating layer is comprised of SiON or SiOC.

3. The method of claim 2, wherein the structure includes a silicon substrate; the conductive layer is comprised of copper; the dielectric layer is comprised of the elements Si, O,

C and/or H; the anti-reflective coating layer is comprised of SiON; and the protective film portion is comprised of C_2H_4 or C_2H_6.

4. The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

5. The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

6. The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

7. The method of claim 1, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

8. The method of claim 1, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; and the protective film portion has a thickness of from about 200 to 1500Å.

9. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer, the protective film portion being comprised of the elements C and H; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening, wherein the via opening process is a dry etch process employing an F-based plasma.

10. The method of claim 1, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 200°C;

pressure: preferably from about 5 to 300 mTorr;

time: preferably from about 10 to 500 seconds; and

plasma power: preferably from about 0 to 3000 W.

11. The method of claim 1, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 100°C;

pressure: preferably from about 5 to 250 mTorr;

time: preferably from about 20 to 300 seconds; and

plasma power: preferably from about 50 to 2500 W.

12. The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer.

13. The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 50 to 2000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

14. The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 100 to

1000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

15. A method of forming a dual damascene opening, comprising the steps of: providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over the exposed portion of the conductive layer and over the etched anti-reflective coating layer; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

16. The method of claim 15, wherein a via plug is formed within the initial via before formation of the trench opening.

17. The method of claim 15, wherein a via plug is formed within the initial via before formation of the trench opening; the via plug being comprised of the elements C, H and/or O.

18. The method of claim 15, wherein the formation of trench opening utilizes a patterned masking layer as a mask.

19. The method of claim 15, wherein the formation of trench opening utilizes a patterned photoresist masking layer as a mask.

20. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer, the protective film portion is being comprised of an organic CVD film; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

21. The method of claim 20, wherein the initial via has a width of from about 200 to 3500Å and the trench opening has a width of from about 5000Å to 100µm.

22. The method of claim 20, wherein the initial via has a width of from about 800 to 2500Å and the trench opening has a width of from about 5000Å to 100µm.

23. A method of forming a dual damascene opening, comprising the steps of:

providing a silicon structure having an overlying exposed conductive layer formed thereover; the conductive layer being comprised of copper, aluminum, gold or silver;

forming a dielectric layer over the exposed conductive layer; the dielectric layer being comprised of the elements Si, O, C and/or H such as SiOCH;

forming an anti-reflective coating layer over the dielectric layer; the anti-reflective coating layer being comprised of SiON or SiOC;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer; the protective film portion being comprised of the elements C and H;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

24. The method of claim 23, wherein the conductive layer is comprised of copper; and the anti-reflective coating layer is comprised of SiON.

25. The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

26. The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

27. The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

28. The method of claim 23, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

29. The method of claim 23, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; and the protective film portion has a thickness of from about 200 to 1500Å.

30. The method of claim 23, wherein the via opening process is a dry etch process employing an F-based plasma.

31. The method of claim 23, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 200°C;

pressure: preferably from about 5 to 300 mTorr;

time: preferably from about 10 to 500 seconds; and

plasma power: preferably from about 0 to 3000 W.

32. The method of claim 23, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 100°C;

pressure: preferably from about 5 to 250 mTorr;

time: preferably from about 20 to 300 seconds; and

plasma power: preferably from about 50 to 2500 W.

33. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer.

34. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 50 to 2000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4 SiOCN, SiOC or SiC.

35. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 100 to 1000Å, and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

36. The method of claim 23, wherein the protective film portion is also formed over the etched anti-reflective coating layer.

37. The method of claim 23, wherein a via plug is formed within the initial via before formation of the trench opening.

38. The method of claim 23, wherein a via plug is formed within the initial via before formation of the trench opening; the via plug being comprised of the elements C, H and/or O.

39. The method of claim 23, wherein the formation of trench opening utilizes a patterned masking layer as a mask.

40. The method of claim 23, wherein the formation of trench opening utilizes a patterned photoresist masking layer as a mask.

41. The method of claim 23, wherein the initial via has a width of from about 200 to 3500Å and the trench opening has a width of from about 5000Å to 100μm.

42. The method of claim 23, wherein the initial via has a width of from about 800 to 2500Å and the trench opening has a width of from about 5000Å. to 100μm.

43. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming an etch stop/liner layer over the exposed conductive layer;

forming a dielectric layer over the etch stop/liner layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the etch stop/liner layer;

removing the exposed portion of the etch stop/liner layer using a liner removal process to expose a portion of the underlying conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

44. The method of claim 43, wherein the structure includes a silicon substrate or a germanium substrate; the conductive layer is comprised of copper, aluminum, gold or silver; the dielectric layer is comprised of the elements Si, O, C and/or H such as SiOCH; the anti-reflective coating layer is comprised of SiON or SiOC; the etch stop/liner layer is comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC; and the protective film portion is comprised of the elements C, H and O.

45. The method of claim 43, wherein the structure includes a silicon substrate; the conductive layer is comprised of copper; the dielectric layer is comprised SiOCH; the anti-reflective coating layer is comprised of SiON; the etch stop/liner layer is comprised of Si_3N_4, SiOCN, SiOC or SiC; and the protective film portion is
comprised of C_2H_4 or C_2H_6.

46. The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

47. The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

48. The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

49. The method of claim 43, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; the etch stop/liner liner

has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

50. The method of claim 43, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; the etch stop/liner liner has a thickness of from about 100 to 1000Å; and the protective film portion has a thickness of from about 200 to 1500Å.